# REDOUBT - RELIABLE FPGA DATAPATH DESIGN USING CONTROL TECHNIQUES, CONTRACT ESA - 4000123993/18/NL/CRS

## Goal of the project

This project proposes a novel control theory inspired fault tolerant methodology for FPGA implementations of processing data-paths working in harsh radiation space environments. The proposed methodology will rely on adding control loops, which will detect and correct the radiation induced faults. We will consider the data-path processing component as a process, for which control components will be added in order to increase the fault tolerance.

The main objectives of this project are:

1. Development of the theoretical background for the control engineering inspired fault tolerant mechanism
2. FPGA implementation for the fault tolerant data-path with control feedback loops
3. Analysis of the proposed methodology in terms of cost and fault tolerance, and comparison with other approaches, such as triple modular redundancy (TMR), reduced precision replicas (RPR), or redundant residue number systems (RRNS).

The proposed technique will target arithmetic dominant applications, which include digital signal processing, robotic arm control, or graphic processing.

## Short description of the project

We aim at providing a novel fault tolerant technique for FPGA based digital electronics used in space applications.

## Project implemented by

Politehnica University Timişoara (UPT) -lead,
Universitatea Tehnică din Cluj-Napoca (UTCN)- project partner.

## Implementation period

July 2018 - June 2019

## Main activities

We will investigate the cost and fault tolerance characteristics of the proposed technique, determining the advantages and the pitfalls. Thus, we will provide the theoretical foundation, a proof-of-concept implementation, as well as guidelines and characteristics for the control based reliability enhancement technique.

The project requires the following four steps:

1. SFI for the target datapath circuit in order to characterize the fault behaviour - This step will require RTL model of the targeted arithmetic intensive circuit, as well as performing the SFI at RTL for the implemented circuit.

2. Analytical modelling for the faulty datapath circuits – This step involves determining the high level modelling of faults, and developing the model associated to the process with perturbations. This step will consist of Matlab simulations.

3. Theoretical controller design used for error correction – In this step, the feedback controller will be designed in order to attenuate and mitigate the perturbations within the process associated to the faulty arithmetic datapath. The controller will be developed in Matlab

4. FPGA implementation and SFI based validation – This step will comprise of the RTL model of the control enhanced fault tolerant circuit, and its evaluation in terms of cost (FPGA implementation cost) and fault tolerance (using SFI). Comparisons with TMR, RRNS and RPR will be performed.

## Results

- We have developed a fault tolerant digital circuit methodology that uses correction feedback loops in order to mitigate the magnitude of errors in data processing circuits.
- The feedback loops implement a linear controller, while the correction process is performed during several iterations.
- The obtained results have indicated that significant cost savings with respect to conventional fault tolerant methodologies, such as TMR, can be obtained.

## Applicability and transferability of the results

- The REDOUBT project has been finalized, with a novel methodology for fault tolerant circuit design, based on control engineering, being developed.

## Financed through/by

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## Research centre

Research Centre for Computers and Information Technology

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